REMARKS

The present Amendment amends claims 1, 3 and 5 and leaves claims 2, 4 and 6 unchanged. Therefore, the present application has pending claims 1-6.

Claims 1-6 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 15, 20, 25, 30, 31 and 37 of U.S. Patent No. 5,133,064; claims 1-6 stand rejected under judicially created doctrine of obviousness type double patenting as being unpatentable over claims 4, 5 and 9 of U.S. Patent No. 6,675,311; claims 1-6 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 5,974,560; and claims 1-6 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 5,542,083. Applicants do not agree with these rejections. However, in order to expedite prosecution of the present application filed on even date herewith is a Terminal Disclaimer obviating these rejections. Therefore, reconsideration and withdrawal of these rejections is respectfully requested.

It should be noted that the filing of the Terminal Disclaimer was not intended nor should it be considered as an agreement on Applicants part that the features recited in claims 1-6 are taught or suggested by the claims of the prior patents. The filing of the Terminal Disclaimer was simply intended to expedite prosecution of the present application.

Claims 1-6 stand rejected under 35 USC §103(a) as being unpatentable over Talbot (U.S. Patent No. 4,689,581) in view of Inmos (EP No. 0 113516). This

rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1-6 are not taught or suggested by Talbot or Inmos whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to claims 1-6 to more clearly recited that the present invention is directed to a memory apparatus formed on one semiconductor substrate. According to the present invention the memory apparatus includes a phase lock loop circuit including a driver, wherein the driver is connected to receive a first clock signal having a first frequency, and the driver generates, based on the first clock signal, a second clock signal which is substantially in phase with the first clock signal and has a second frequency, a memory part which stores data, and an interface circuit. The interface circuit, in synchronism with said second clock signal, outputs the data.

The above described features of the present invention as now more clearly recited in claims 1-6 are not taught or suggested by any of the references of record, particularly Talbot and Inmos whether taken individually or in combination with each other as suggested by the Examiner.

Talbot teaches an integrated circuit device having a timing apparatus arranged to produce timing signals whose frequency is a multiple of that of a clock signal. The timing apparatus taught by Talbot, including a phase locked loop, is formed on a single chip and no external components are necessary. The phase locked loop includes a convertor and filter circuit, the convertor including two

transistor current sources whose current magnitude is determined by a current reference circuit including current mirror transistors. The current sources are controlled by increase and decrease output signals from a phase and frequency comparator such that the output of the convertor depends upon the mark space ratio of the comparator output signals. The output of the convertor as per Talbot is filtered and then fed as a control voltage to a voltage controlled oscillator. The oscillator output is fed by way of a divider to the phase comparator and also provides the high frequency input timing signal for a logic device, such as a microcomputer.

The above described teachings of Talbot do not teach or suggest the features of the present invention regarding the use of a driver to receive a first clock signal having a first frequency, and to generate, based on the first clock signal, a second clock signal which is substantially in phase with the first clock signal and a has a second frequency as in the present invention. By use of the driver according to the present invention the phase lock loop is able to supply a high quality clock signal having a complete clock pulse width (duty) not possible in conventional phase lock loops as taught by Talbot.

Thus, Talbot fails to teach or suggest a phase lock loop circuit including a driver, wherein the driver is connected to receive a first clock signal having a first frequency, and the driver generates, based on the first clock signal, a second clock signal which is substantially in phase with the first clock signal and has a second frequency as recited in the claims.

Therefore, as is quite clear from the above, Talbot fails to teach or suggest numerous features of the present invention as now more clearly recited in the claims.

The above described deficiencies of Talbot are not supplied by Inmos. Accordingly, combining the teachings of Talbot and Inmos in the manner suggested by the Examiner in the Office Action still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

The Examiner merely relies on Inmos for an alleged teaching of the inclusion of a memory as a logic device. However, this alleged teaching of Inmos does not supply the above noted deficiencies of Talbot relative to the features of the present invention as now recited in the claims. Particularly Inmos does not teach or suggest the use of a driver to receive a first clock signal having a first frequency, and to generate, based on the first clock signal, a second clock signal which is substantially in phase with the first clock signal and a has a second frequency as in the present invention.

Thus, Inmos fails to teach or suggest a phase lock loop circuit including a driver, wherein the driver is connected to receive a first clock signal having a first frequency, and the driver generates, based on the first clock signal, a second clock signal which is substantially in phase with the first clock signal and has a second frequency as recited in the claims.

Therefore, as is clear from the above, both Talbot and Inmos suffer from the same deficiencies relative to the features of the present invention as now more clearly recited in the claims and as such combining Talbot and Inmos in the manner suggested by the Examiner in the Office Action does not render obvious the features of the present invention as now more clearly recited in the claims. Accordingly,

reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 1-6 as being unpatentable over Talbot in view of Inmos is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-6.

In view of the foregoing amendments and remarks, applicants submit that claims 1-6 are in condition for allowance. Accordingly, early allowance of claims 1-6 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (501.25958CV7).

Respectfully submitted,

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